Claims

What is claimed is:

1. A microelectronic package comprising:

a first level substrate including a plurality of microelectronic devices and a plurality of first level substrate input/output pads in a face thereof;

a thin film decal on the face of the first level substrate, the thin film decal including first and second opposing faces, a plurality of first decal input/output pads on the first face, at least one of which is electrically connected to at least one of the first level substrate input/output pads, a plurality of second decal input/output pads on the second face and at least one internal wiring layer that is electrically connected to at least one of the first and second decal input/output pads;

a second level substrate including a plurality of second level substrate input/output pads on a face thereof; and

a dielectric adhesive layer that is adhesively bonded to the thin film decal and that is adhesively boded to the second level substrate, the dielectric adhesive layer including a plurality of conductive vias therein that electrically connect at least one of the second level substrate input/output pads to at least one of the second decal input/output pads.

2 A microelectronic package according to Claim 1 wherein the conductive vias comprise conductive adhesive vias.

3. A microelectronic package according to Claim 1 wherein the first level substrate is an integrated circuit and wherein the second level substrate is a printed circuit board.

4. A microelectronic package according to Claim 2 wherein the conductive vias are screened conductive adhesive vias.

5. A microelectronic package according to Claim 1 further comprising a stress buffer layer in the dielectric adhesive layer.

6. A microelectronic package according to Claim 1 wherein the first face includes a rippled surface.

7. A microelectronic package according to Claim 1 wherein the first face is substantially planar and topography-free.

8. A microelectronic package according to Claim 1 wherein the thin film decal and the dielectric adhesive layer collectively comprises a Planar Graft Patch that is grafted onto said second level substrate from a process substrate.

9. A microelectronic package comprising:

a substrate;

a release layer on the substrate;

a thin film decal on the release layer, opposite the substrate, the thin film decal including first and second opposing faces, a plurality of first decal input/output pads on the first face, and a plurality of second decal input/output pads in the second face and at least one internal wiring layer that is electrically connected to at least one of the first and second decal input/output pads; and

a dielectric adhesive layer that is adhesively bonded to the thin film decal, the dielectric adhesive layer including a plurality of conductive vias therein that electrically connect to at least one of the second decal input/output pads.

10. A microelectronic package according to Claim 9 wherein the conductive vias comprise conductive adhesive vias.

11. A microelectronic package according to Claim 9 wherein the substrate is a glass substrate.

12. A microelectronic package according to Claim 9 wherein the conductive vias are screened conductive adhesive vias.

13. A microelectronic package according to Claim 9 further comprising a stress buffer layer in the dielectric adhesive layer.

14. A microelectronic package according to Claim 9 wherein the first face includes a rippled surface.

15. A microelectronic package according to Claim 9 wherein the first face is substantially planar and topography-free.